VAC Number	FY22 E22

Job Description

Job Title:	Digital IF FPGA Engineer
Responsible to:	Head of Software
Department (s):	Engineering

JOB PURPOSE

As part of a small team within ETL's engineering department, to specify, develop and design a new range of cutting edge digital IF distribution products.

ROLE DIMENSIONS

Working as a part of a small team, reporting to Digital RF Team Lead

The role will suit someone with a strong background in network protocols, and a working knowledge of communications systems engineering and digital signal processing. You will probably have worked in software radio, or related discipline. A pragmatic approach to the implementation of FPGA based network equipment is essential. Ideally, you will have worked with SoC FPGAs such as Zynq or Cyclone device families.

You will be responsible for implementing VITA-49 or similar network SDR transport protocols. You will have excellent FPGA skills, including working on mid-sized to large designs where there are multiple code authors. You will take sampled and processed signals from the DSP blocks implemented by the DSP engineer and efficiently packetize and add context for data transmission over ethernet. You will be able to size FPGA processing requirements, and have a working knowledge of the benefits of leading FPGA devices.

You will be working on cutting edge technology as part of a multidisciplinary team in a fast-paced environment. You will rapidly gain skills in all technologies present in a complex digitization product line, working on some of the most complex and powerful FPGAs on the market today.

KEY RESPONSIBILITIES AND ACCOUNTABILITIES

- To design and develop a range of modules and equipment for digital IF
- Integration and test of digital IF equipment
- Produce VHDL code for VITA-49 or similar network SDR transport protocols
- Scripting in TCL designs utilizing IP Cores for rapid development
- Build scripting to support continuous integration
- Design and development of test benches to prove VHDL code
- Conduct floor-planning and timing analysis of designs, achieving timing closure
- Test of VHDL code on target platform
- Integration of firmware into application design

COMPETENCIES REQUIRED FOR THE ROLE		
Qualifications and Experience	**Essential (E) or Desirable**	**HR Office Use Only**
Previous Industry experience and, or direct experience of MPSoC Parts	E	
Experience of SDR protocols such as VITA-49	E	
Experience of FPGA implementation of communications stacks including TCP/IP	E	
Extensive experience of FPGA synthesis tools such as Synplify, Vivado, Quartus or Mentor	E	
Extensive experience of writing FPGA test benches	E	
Experience of DSP Algorithm simulation in MATLAB / Python	D	
Understanding of data-converter specifications and error sources	D	
Efficient implementation of DSP algorithms in VHDL	D	
Experience of high speed mixed signal PCB design constraints	D	
Skills		
FPGA code design, synthesis, implementation and test	E	
Build scripting for reproducible builds in a team environment	E	
Experience in C / C++ / Rust or other high level language	D	
Experience of working in an Agile Test Driven environment	D	
Team player, good communication skills, excellent attention to detail	E	
Personal Qualities		
Professional business attire, professional and approachable manner	E	
The ability to develop excellent working relationships	E	
Positive, confident and enthusiastic attitude at all times	E	
Flexible and adaptable to fast paced changing environments	E	
Passionate and keen interest in manufacturing techniques	D	
Ability to attend conferences, exhibitions, seminars, networking events outside of working hours	D	

JOB DESCRIPTION AGREEMENT	
We confirm that this conveys a full and accurate description of the job as at November 2021	
Job Holder's Signature:	Date:
Manager of Department Signature: 	Date:4/11/21
Director of Department Signature:	Date: